CLAIMS

What is claimed is:

1. A switching device comprising:

at least two base racks, each base rack including

a line card having at least one port capable of receiving and transmitting a packet;

a switch card in communication with the line card across a backplane;

the at least two base racks coupled such that the switch cards of each base rack are in communication.

2. The switching device of claim 1 wherein each base rack includes 16 line cards and 4 switch cards, and wherein each line card includes 16 ports.

3. The switching device of claim 2 wherein each switch card of each base rack is in communication with each switch card of each other base rack.

4. The switching device of claim 1 wherein the at least two base racks comprise four base racks, and wherein each base rack includes 16 line cards and 4 switch cards, and wherein each line card includes 16 ports.

5. The switching device of claim 4 wherein each switch card of each base rack is in communication with each switch card of each other base rack.

6. The switching device of claim 1 wherein each base rack includes 4 line cards and 2 switch cards, and wherein each line card includes 16 ports.

7. The switching device of claim 6 wherein each switch card of each base rack is in communication with each switch card of each other base rack.

8. The switching device of claim 1 wherein the at least two base racks comprise four base racks, and wherein each base rack includes 4 line cards and 2 switch cards, and wherein each line card includes 16 ports.

9. The switching device of claim 8 wherein each switch card of each base rack is in communication with each switch card of each other base rack.

10. The switching device of claim 1 wherein each line card further includes a PHY chip and a packet processing ASIC connected in series between the at least one port and the backplane.

11. The switching device of claim 10 wherein coupled to the packet processing ASIC is an SRAM and a network processor unit coupled to a DRAM.

12. The switching device of claim 1 wherein each switch card further includes a flow control ASIC coupled to the backplane.

13. The switching device of claim 12 wherein the flow control ASIC is further coupled to a GBIC coupled to a cascade port.

14. The switching device of claim 12 wherein the flow control ASIC is coupled to the backplane with four input/output links.

15. A switching device comprising:

a first base rack including

a first line card having a first port capable of receiving a packet;

a first switch card in communication with the first line card;

a second base rack including

a second line card having a second port capable of transmitting a packet;

a second switch card in communication with the second line card, and in further communication with the first switch card.

16. The switching device of claim 15 wherein the first base rack and the second base rack each include 16 line cards and 4 switch cards, and wherein each line card includes 16 ports.

17. The switching device of claim 16 wherein each switch card of the first base rack is in communication with each switch card of the second base rack.

18. The switching device of claim 15 wherein the first base rack and the second base rack each include 4 line cards and 2 switch cards, and wherein each line card includes 16 ports.

19. The switching device of claim 18 wherein each switch card of the first base rack is in communication with each switch card of the second base rack.

20. The switching device of claim 15 wherein the first line card further includes a first PHY chip and a first packet processing ASIC connected in series between the first port and a first backplane, and wherein the second line card further includes a second PHY chip and a second packet processing ASIC connected in series between the second port and a second backplane.

21. The switching device of claim 20 wherein coupled to each packet processing ASIC is an SRAM and a network processor unit coupled to a DRAM.

22. The switching device of claim 15 wherein the first switch card further includes a first flow control ASIC coupled to a first backplane, and wherein the second switch card further includes a second flow control ASIC coupled to a second backplane.

23. The switching device of claim 22 wherein the first switch card further includes the first flow control ASIC coupled to a first GBIC coupled to a first cascade port, and wherein the second switch card further includes the second flow control ASIC coupled to a second GBIC coupled to a second cascade port.

24. The switching device of claim 22 wherein the first flow control ASIC is coupled to the first backplane with four input/output links, and wherein the second flow control ASIC is coupled to the second backplane with four input/output links.

25. A switching device comprising:

a first base rack including

a first line card having an ingress port capable of receiving a packet, the first line card being capable of processing the packet;

a first switch card in communication with the first line card and capable of accepting the packet therefrom, the first switch card including a first cascade port, the first switch card capable of routing the packet to the first cascade port;

a second base rack including

a second line card including an egress port, the second line card being capable of processing the packet and further capable of sending the packet to the egress port, the egress port being capable of transmitting the packet;

a second switch card including a second cascade port coupled to the first cascade port, the second switch card being capable of receiving the packet from the first cascade port via the second cascade port, the second switch card being in communication with the second line card and capable of routing the packet thereto.

26. The switching device of claim 25 wherein each base rack includes 16 line cards and 4 switch cards, and wherein each line card of the first base rack includes 16 ingress ports, and each line card of the second base rack includes 16 egress ports.

27. The switching device of claim 26 wherein each first switch card of the first base rack is in communication with each second switch card of the second base rack.

28. The switching device of claim 25 wherein each base rack includes 4 line cards and 2 switch cards, and wherein each line card of the first base rack includes 16 ingress ports, and each line card of the second base rack includes 16 egress ports.

29. The switching device of claim 28 wherein each first switch card of the first base rack is in communication with each second switch card of the second base rack.

30. The switching device of claim 25 wherein the first line card of the first base rack further includes a first PHY chip and a first packet processing ASIC connected in series between the ingress port and a first backplane, and wherein the second line card of the second base rack further includes a second PHY chip and a second packet processing ASIC connected in series between the egress port and a second backplane.

31. The switching device of claim 30 wherein coupled to each packet processing ASIC is an SRAM and a network processor unit coupled to a DRAM.

32. The switching device of claim 25 wherein the first switch card further includes a first flow control ASIC coupled to a first backplane, and wherein the second switch card further includes a second flow control ASIC coupled to a second backplane.

33. The switching device of claim 32 wherein the first flow control ASIC is further coupled to a first GBIC coupled to the first cascade port, and wherein the second flow control ASIC is further coupled to a second GBIC coupled to the second cascade port.

34. The switching device of claim 32 wherein the first flow control ASIC is coupled to the first backplane with four input/output links, and wherein the second flow control ASIC is coupled to the second backplane with four input/output links.

35. The switching device of claim 25 wherein the ingress and egress ports are bi-directional.

36. The switching device of claim 25 wherein the capability of processing the packet in the first line card includes converting the packet from an optical signal to an electrical signal and segmenting the packet to one or more cells, and wherein the capability processing the packet in the second line card includes reassembling the one or more cells back to the packet and converting the packet from an electrical signal to an optical signal.

37. A system area network comprising:

a switching device including

a first base rack including

a first line card having an ingress port capable of receiving a packet, the first line card being capable of processing the packet;

a first switch card in communication with the first line card and capable of accepting the packet therefrom, the first switch card including a first cascade port, the first switch card capable of routing the packet to the first cascade port;

a second base rack including

a second line card including an egress port, the second line card being capable of processing the packet and further capable of sending the packet to the egress port, the egress port being capable of transmitting the packet;

a second switch card including a second cascade port coupled to the first cascade port, the second switch card being capable of receiving the packet from the first cascade port via the second cascade port, the second switch card being in communication with the second line card and capable of routing the packet thereto;

a storage device coupled to the ingress port; and

a server coupled to the egress port.

38. The system area network of claim 37 wherein each base rack includes 16 line cards and 4 switch cards, and wherein each line card of the first base rack includes 16 ingress ports, and each line card of the second base rack includes 16 egress ports.

39. The system area network of claim 38 wherein each first switch card of the first base rack is in communication with each second switch card of the second base rack.

40. The system area network of claim 37 wherein each base rack includes 4 line cards and 2 switch cards, and wherein each line card of the first base rack includes 16 ingress ports, and each line card of the second base rack includes 16 egress ports.

41. The system area network of claim 40 wherein each first switch card of the first base rack is in communication with each second switch card of the second base rack.

42. The system area network of claim 37 wherein the first line card of the first base rack further includes a first PHY chip and a first packet processing ASIC connected in series between the ingress port and a first backplane, and wherein the second line card of the second base rack further includes a second PHY chip and a second packet processing ASIC connected in series between the egress port and a second backplane.

43. The system area network of claim 42 wherein coupled to each packet processing ASIC is an SRAM and a network processor unit coupled to a DRAM.

44. The system area network of claim 37 wherein the first switch card further includes a first flow control ASIC coupled to a first backplane, and wherein the second switch card further includes a second flow control ASIC coupled to a second backplane.

45. The system area network of claim 44 wherein the first flow control ASIC is further coupled to a first GBIC coupled to the first cascade port, and wherein the second flow control ASIC is further coupled to a second GBIC coupled to the second cascade port.

46. The system area network of claim 44 wherein the first flow control ASIC is coupled to the first backplane with four input/output links, and wherein the second flow control ASIC is coupled to the second backplane with four input/output links.

47. The system area network of claim 37 further comprising an IP router and an IP switch.

48. The system area network of claim 37 wherein the storage device includes a RAID.

49. The system area network of claim 37 wherein the storage device includes a JBOD.

50. The system area network of claim 37 wherein the storage device includes a tape backup.

51. A method for switching a packet comprising:

introducing a packet into a first port of a first line card of a first base rack;

transmitting the packet from the first line card through a first backplane to a first switch card of the first base rack;

transmitting the packet from the first switch card to a second switch card of a second base rack;

transmitting the packet from the second switch card through a second backplane to a second line card on the second base rack; and

transmitting the packet out of a second port of the second base rack.

52. The method of claim 51 wherein transmitting the packet from the first switch card to the second switch card includes reading a second port number and determining the second port number is associated with the second base rack.

53. The method of claim 51 wherein transmitting the packet from the first switch card to the second switch card includes transmitting the packet from a first cascade port on the first switch card to a second cascade port on the second switch card.

54. The method of claim 53 wherein transmitting the packet from the first switch card to the second switch card further includes transmitting the packet across a connector joining the first and second cascade ports.

55. The method of claim 54 wherein the connector between the first and second cascade ports includes an optical fiber and wherein transmitting the packet from the first cascade port to the second cascade port includes converting the packet to an optical signal.

56. The method of claim 55 wherein transmitting the packet from the first switch card to the second switch card further includes buffering the packet on the second switch card.

57. The method of claim 51 wherein introducing the packet into the first port of the first line card includes converting the packet from an optical signal to an electrical signal.

58. The method of claim 57 wherein introducing the packet into the first port of the first line card further includes performing a physical layer conversion.

59. The method of claim 58 wherein introducing the packet into the first port of the first line card further includes performing fast-path packet processing.

60. The method of claim 58 wherein introducing the packet into the first port of the first line card further includes performing slow-path packet processing.

61. The method of claim 51 wherein transmitting the packet through the first backplane includes segmenting the packet into at least one cell.

62. The method of claim 61 wherein segmenting the packet creates a payload of 64 bytes.

63. The method of claim 61 wherein segmenting the packet creates a payload of 128 bytes.

64. The method of claim 61 wherein segmenting the packet further includes staging packet data at an SRAM, waiting for packet header processing to be completed, placing a request for first backplane arbitration into a priority queue, winning first backplane arbitration, and reading packet data from the SRAM.

65. The method of claim 61 wherein segmenting the packet additionally includes reading a cell-size from an SRAM and high-speed serial transmission of the at least one cell across the first backplane to the first switch card.

66. The method of claim 65 wherein segmenting the packet additionally includes placing the at least one cell in a buffer on a first FLC on the first switch card.

67. The method of claim 51 wherein transmitting the packet through the second backplane includes placing the packet in a priority output queue on the second switch card.

68. The method of claim 67 wherein transmitting the packet through the second backplane further includes scheduling to use the second port.

69. The method of claim 68 wherein transmitting the packet through the second backplane further includes sending the packet from a first FLC to a crossbar, routing the packet through the crossbar, and buffering the packet at an egress buffer on a second FLC.

70. The method of claim 69 wherein transmitting the packet through the second backplane further includes determining a credit at a receiving queue on the second line card and high-speed serial transmission of the packet across the second backplane.

71. The method of claim 51 wherein transmitting the packet out of a second port of the second base rack includes processing the packet by the second line card.

72. The method of claim 71 wherein processing the packet includes reassembling at least one cell into the packet.

73. The method of claim 71 wherein processing the packet further includes performing a physical layer conversion.

74. The method of claim 71 wherein processing the packet further includes converting the packet from an electrical signal to an optical signal.

75. The method of claim 51 wherein transmitting the packet from the first line card includes buffering the packet in a set of queues associated with a packet processor on the line card.

76. The method of claim 51 wherein transmitting the packet to the first switch card includes buffering the packet in a set of queues associated with a flow control ASIC on the switch card.

77. The method of claim 51 wherein transmitting the packet from the first switch card to the second switch card includes routing the packet through a crossbar on the first switch card and buffering the packet in a first queue dedicated to a cascade port on the first base rack.

78. The method of claim 77 wherein transmitting the packet from the first switch card to the second switch card further includes buffering the packet in a second queue associated with a flow control ASIC on the second switch card.

79. The method of claim 51 wherein transmitting the packet from the second switch card through the second backplane includes routing the packet through a crossbar on the second switch card and buffering the packet in a queue between the crossbar and the second backplane.

80. The method of claim 51 wherein transmitting the packet through the second backplane to a second line card includes buffering the packet in a queue on the second line card dedicated to a destination port.